

1/4 DUTY LCD DRIVER

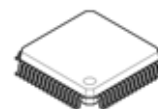
■ GENERAL DESCRIPTION

The NJU6433B is a 1/4 duty LCD driver for segment type LCD panel.

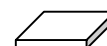
The LCD driver consists of 4-common and 50-segment drives up to 200 segments.

The NJU6433B is useful for the digital tuning system or others segment type display driver.

■ PACKAGE OUTLINE



NJU6433BFH1

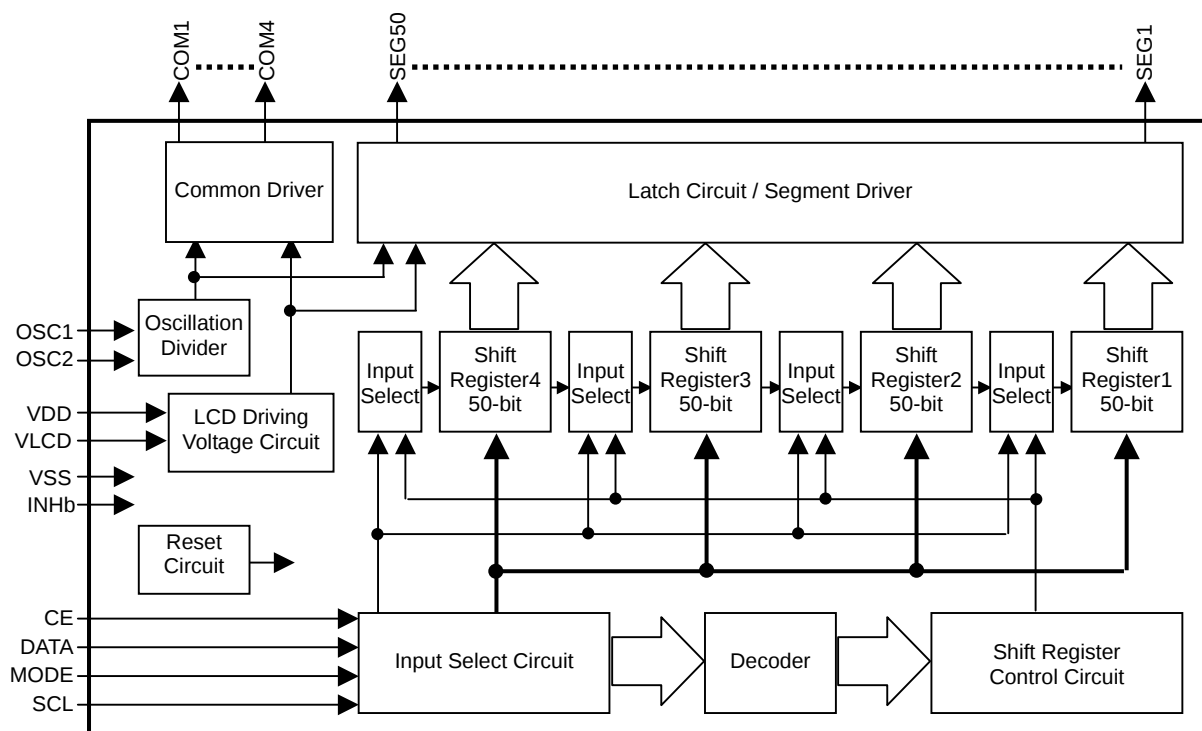


NJU6433BC

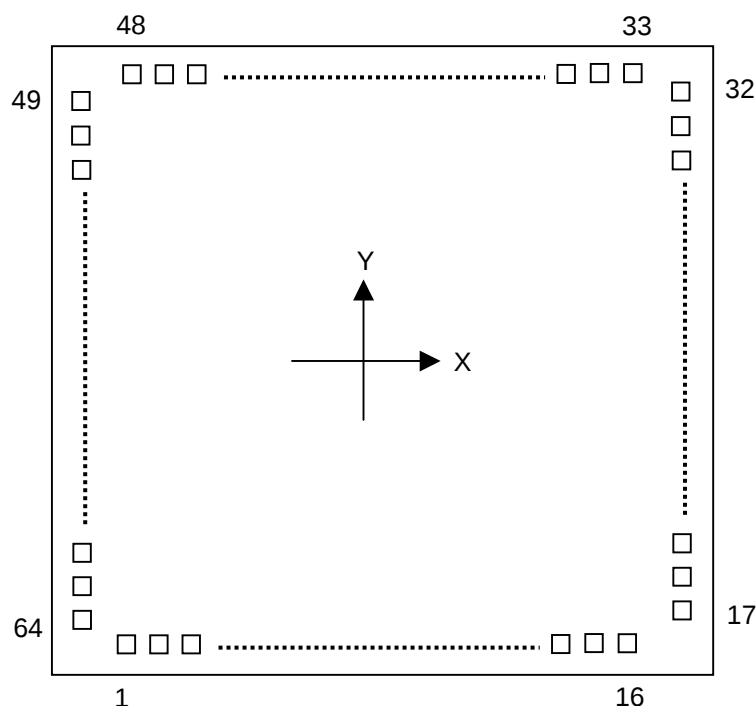
■ FEATURES

- 50 Segment Drivers
- Duty Ratio 1/4 (Up to 200-Segments)
- Serial Data Transmission (Shift Clock 2MHz max.)
- Oscillation Circuit On-chip (External Resistance Required)
- Display Off Function (INHb Terminal)
- Operating Voltage 2.4 to 5.5V
- LCD Driving Voltage 6.5V Max.
- Package Outline Chip, QFP64-H1
- C-MOS Technology

■ BLOCK DIAGRAM



■ PAD LOCATION



Chip Center : X=0 μ m, Y=0 μ m
 Chip Size : X=3.20 mm, Y=3.20 mm
 Chip Thickness : 400 μ m
 PAD Size : X=99.2 μ m, Y=99.2 μ m
 PAD Pitch : 171.2 μ m

■ PAD COORDINATES

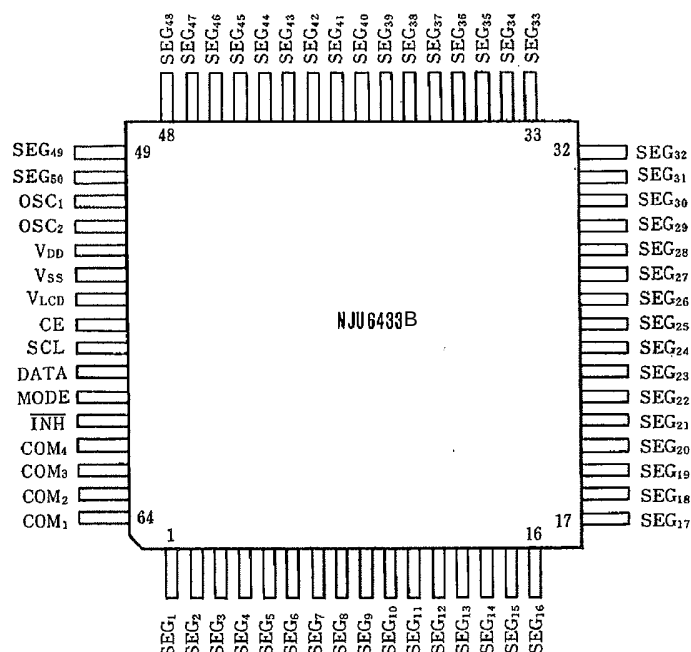
Chip Size 3.20 x 3.20 mm(Chip Center X=0 μ m, Y=0 μ m)

PAD No.	Terminal	X= μ m	Y= μ m
1	SEG ₁	-1279	-1437
2	SEG ₂	-1107	-1437
3	SEG ₃	-936	-1437
4	SEG ₄	-765	-1437
5	SEG ₅	-594	-1437
6	SEG ₆	-423	-1437
7	SEG ₇	-251	-1437
8	SEG ₈	-80	-1437
9	SEG ₉	91	-1437
10	SEG ₁₀	262	-1437
11	SEG ₁₁	433	-1437
12	SEG ₁₂	605	-1437
13	SEG ₁₃	776	-1437
14	SEG ₁₄	947	-1437
15	SEG ₁₅	1118	-1437
16	SEG ₁₆	1289	-1437
17	SEG ₁₇	1437	-1288
18	SEG ₁₈	1437	-1117
19	SEG ₁₉	1437	-946
20	SEG ₂₀	1437	-775
21	SEG ₂₁	1437	-603
22	SEG ₂₂	1437	-432
23	SEG ₂₃	1437	-261
24	SEG ₂₄	1437	-90

PAD No.	Terminal	X= μ m	Y= μ m
25	SEG ₂₅	1437	81
26	SEG ₂₆	1437	253
27	SEG ₂₇	1437	424
28	SEG ₂₈	1437	595
29	SEG ₂₉	1437	766
30	SEG ₃₀	1437	937
31	SEG ₃₁	1437	1109
32	SEG ₃₂	1437	1280
33	SEG ₃₃	1280	1437
34	SEG ₃₄	1109	1437
35	SEG ₃₅	937	1437
36	SEG ₃₆	766	1437
37	SEG ₃₇	595	1437
38	SEG ₃₈	424	1437
39	SEG ₃₉	253	1437
40	SEG ₄₀	81	1437
41	SEG ₄₁	-90	1437
42	SEG ₄₂	-261	1437
43	SEG ₄₃	-432	1437
44	SEG ₄₄	-603	1437
45	SEG ₄₅	-775	1437
46	SEG ₄₆	-946	1437
47	SEG ₄₇	-1117	1437
48	SEG ₄₈	-1288	1437

PAD No.	Terminal	X= μ m	Y= μ m
49	SEG ₄₉	-1437	1280
50	SEG ₅₀	-1437	1109
51	OSC ₁	-1437	937
52	OSC ₂	-1437	766
53	V _{DD}	-1437	595
54	V _{SS}	-1437	424
55	V _{LCD}	-1437	253
56	CE	-1437	81
57	SCL	-1437	-90
58	DATA	-1437	-261
59	MODE	-1437	-432
60	INHX	-1437	-603
61	COM ₄	-1437	-775
62	COM ₃	-1437	-946
63	COM ₂	-1437	-1117
64	COM ₁	-1437	-1288

PIN CONFIGURATION



TERMINAL DESCRIPTION

No.	SYMBOL	FUNCTION
1~50	SEG ₁ ~SEG ₅₀	LCD Segment Output Terminals
61~64	COM ₄ ~COM ₁	LCD Common Output Terminals
51	OSC ₁	Oscillation Terminals : External resistance is connected to these terminals.
52	OSC ₂	
53	V _{DD}	Power Supply (+5V)
54	V _{SS}	Power Supply (0V)
55	V _{LCD}	Power Supply for LCD Driving The relation : $1.3V_{DD} \geq V_{DD} - V_{LCD} $, $V_{SS} \geq V_{LCD}$ must be maintained.
56	CE	Chip Enable Signal Input Terminal : "H" : LCD display data and mode setting data input "L" : Disable Fall Edge : LCD display data latch
57	SCL	Serial Data Transmission Clock Input Terminal : LCD display and Mode setting data are input synchronized SCL clock signal rise edge.
58	DATA	Serial Data Input Terminal Data input timing : SCL clock rise edge
59	MODE	Data or Mode Select Terminal "H" : Data input mode "L" : LCD display data input mode (Refer the mode setting table for mode setting contents)
60	INHb	Display-Off Control Terminal : When display goes to off, the display data in the shift-register is retained. "H" : Display-On "L" : Display-Off

■ FUNCTIONAL DESCRIPTION

(1) Operation of each block

(1-1) Oscillation Circuit

The oscillation circuit operates by connecting external resistance (capacitance is incorporated). This circuit provides the clock signal to both common and segment drivers.

(1-2) Divider Circuit

This circuit divides the oscillating signal to generate the common and segment timing.

(1-3) Shift-Register

When the CE terminal is "H" (Enable mode), the display data is transferred to the shift-register synchronized by the shift clock on the SCL terminal.

(1-4) Latch Circuit and Segment Driver

When the CE signal falling, the display data is latched, and the data controls the segment signal of display-on/off.

(1-5) Common Driver

The Common driver generates driving waveform to common terminal.

(1-6) Reset Circuit

The Reset circuit is type of detectable voltage. It resets internal circuit when the power turns on.

(2) Mode Setting

The mode setting is composed of 4-bit, and selects the shift register that writes the display data by writing data in the mode setting register. (Refer to "(4) Data Input Timing" for details.)

When the data (1,1,1,1) is input, "0" (All Display-off) is written in all shift registers.

The mode setting register is selected by CE="H" and MODE="H". The data is latched at the rising edge of the SCL, and selected at falling edge of the CE.

Table 1. Mode Setting Table

Mode	Data	Description
1	(MSB) 1,0,0,0 (LSB)	Shift register 1 is selected.
2	0,1,0,0	Shift register 2 is selected.
3	1,1,0,0	Shift register 3 is selected.
4	0,0,1,0	Shift register 4 is selected.
5	1,0,1,0	All Shift register (1~4) is selected, and data is written continuously.
F	1,1,1,1	All shift register is "0".

(3) Correspondence of the transfer data and output terminal

The display data is written by CE="H" and MODE="L". The data is latched at the rising edge of the SCL, and written at falling edge of the CE.

The correspondence of the data and the output terminals is as follows.

Output Terminal	COM ₁	COM ₂	COM ₃	COM ₄
SEG ₁	D1	D2	D3	D4
SEG ₂	D5	D6	D7	D8
SEG ₃	D9	D10	D11	D12
SEG ₄	D13	D14	D15	D16
SEG ₅	D17	D18	D19	D20
SEG ₆	D21	D22	D23	D24
SEG ₇	D25	D26	D27	D28
SEG ₈	D29	D30	D31	D32
SEG ₉	D33	D34	D35	D36
SEG ₁₀	D37	D38	D39	D40
SEG ₁₁	D41	D42	D43	D44
SEG ₁₂	D45	D46	D47	D48
SEG ₁₃	D49	D50	D51	D52
SEG ₁₄	D53	D54	D55	D56
SEG ₁₅	D57	D58	D59	D60
SEG ₁₆	D61	D62	D63	D64
SEG ₁₇	D65	D66	D67	D68
SEG ₁₈	D69	D70	D71	D72
SEG ₁₉	D73	D74	D75	D76
SEG ₂₀	D77	D78	D79	D80
SEG ₂₁	D81	D82	D83	D84
SEG ₂₂	D85	D86	D87	D88
SEG ₂₃	D89	D90	D91	D92
SEG ₂₄	D93	D94	D95	D96
SEG ₂₅	D97	D98	D99	D100

Output Terminal	COM ₁	COM ₂	COM ₃	COM ₄
SEG ₂₆	D101	D102	D103	D104
SEG ₂₇	D105	D106	D107	D108
SEG ₂₈	D109	D110	D111	D112
SEG ₂₉	D113	D114	D115	D116
SEG ₃₀	D117	D118	D119	D120
SEG ₃₁	D121	D122	D123	D124
SEG ₃₂	D125	D126	D127	D128
SEG ₃₃	D129	D130	D131	D132
SEG ₃₄	D133	D134	D135	D136
SEG ₃₅	D137	D138	D139	D140
SEG ₃₆	D141	D142	D143	D144
SEG ₃₇	D145	D146	D147	D148
SEG ₃₈	D149	D150	D151	D152
SEG ₃₉	D153	D154	D155	D156
SEG ₄₀	D157	D158	D159	D160
SEG ₄₁	D161	D162	D163	D164
SEG ₄₂	D165	D166	D167	D168
SEG ₄₃	D169	D170	D171	D172
SEG ₄₄	D173	D174	D175	D176
SEG ₄₅	D177	D178	D179	D180
SEG ₄₆	D181	D182	D183	D184
SEG ₄₇	D185	D186	D187	D188
SEG ₄₈	D189	D190	D191	D192
SEG ₄₉	D193	D194	D195	D196
SEG ₅₀	D197	D198	D199	D200

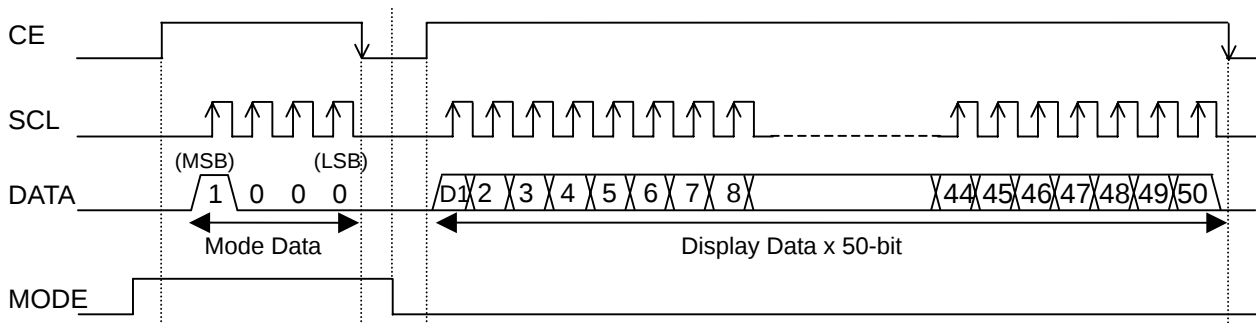
Correspondence of the transfer data and Segment Status

Transfer Data	Segment Status
"H"	ON
"L"	OFF

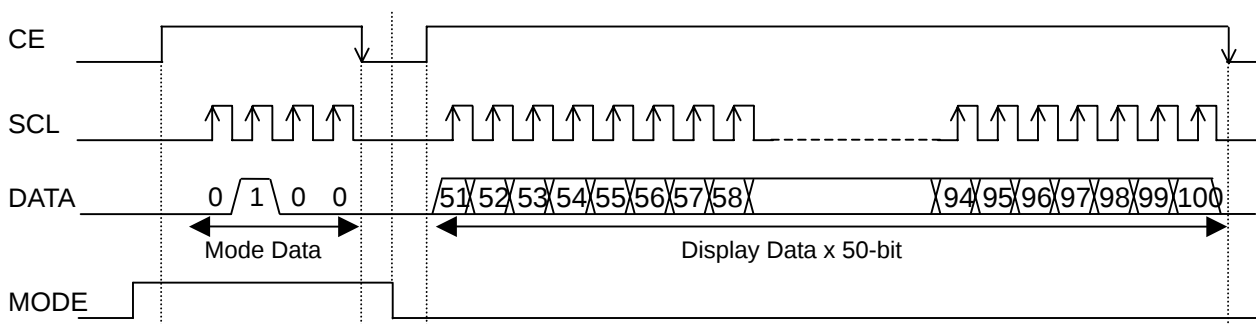
(4) Data Input Timing

The format of data is as follows. The mode data is input by 4-bit of MSB first, and after the shift register is selected, the display data is written

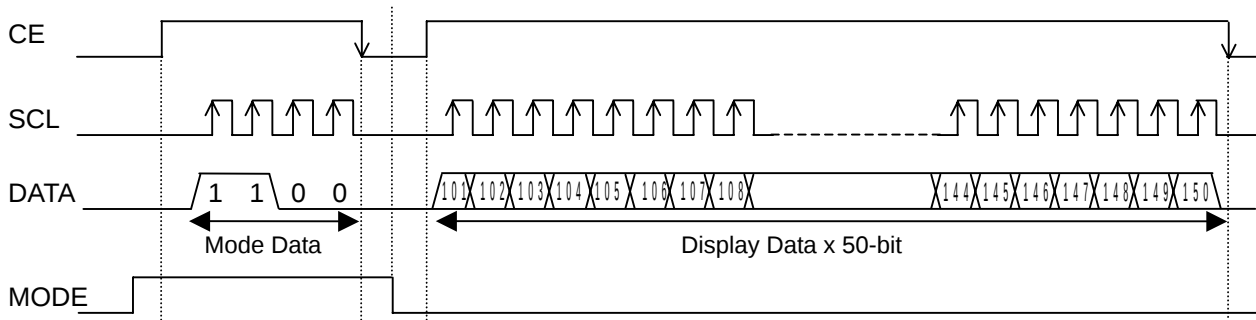
- Mode 1 : Shift Register 1 (D1~D50)



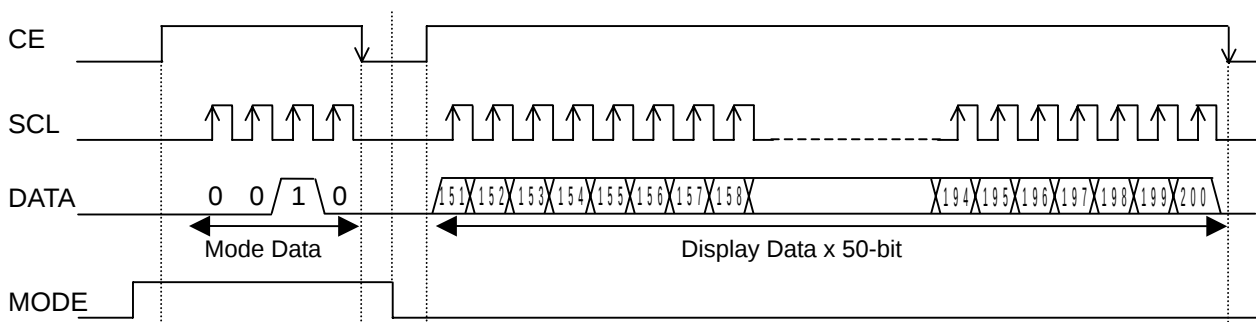
- Mode 2 : Shift Register 2 (D51~D100)



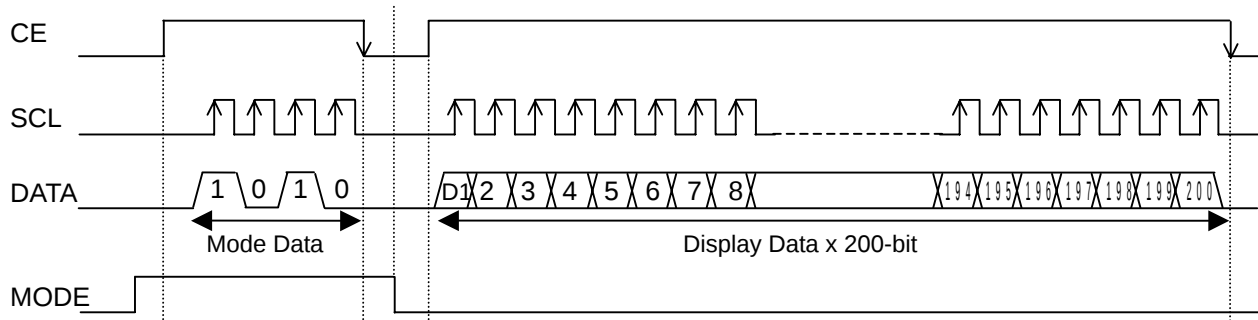
- Mode 3 : Shift Register 3 (D101~D150)



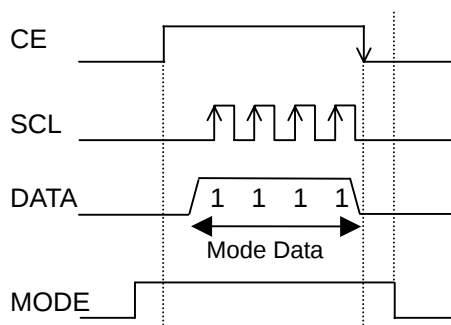
- Mode 4 : Shift Register 4 (D151~D200)



- Mode 5 : Shift Register 1~4 (D1~D200)



- Mode F : Shift Register 1~4 all "0"



Note 1) All of display data should be transmitted within 30ms to keep the display quality, because huge display data D1 to D200 are transmitted at 4 times totally.

Note 2) Data is latched at the rising edge of the SCL.

Note 3) Mode data and display data are executed at the falling edge of the CE.

Note 4) In case of less than 4-bit data, the mode data remains the LSB side of the previous mode data.

Note 5) In case of over 4-bit data, the mode data is valid the previous 4-bit of the falling edge of the CE.

Note 6) In case of less than 50-bit data, the display data remains the last part of the previous display data.

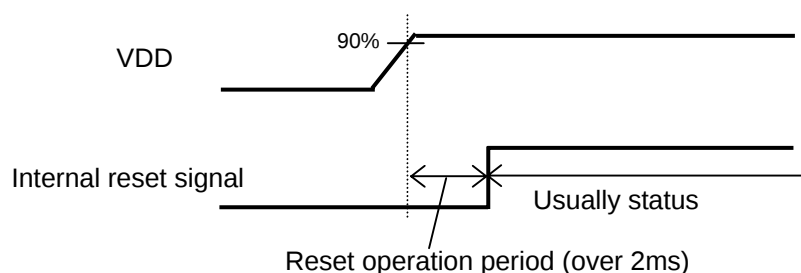
Note 7) In case of over 50-bit data, the display data is valid the previous 50-bit of the falling edge of the CE.

(5) Initialization by Power On Reset

The **NJU6433B** incorporates the reset circuit of the detectable voltage type, and when the power supply is turned on, it automatically initializes it (reset). When the VDD becomes 90% of the working voltage, the reset signal is generated internally. Reset is completed after 2ms, and it becomes usually status. The serial data is able to transmit after completed reset.

(5-1) Status of Power On Reset

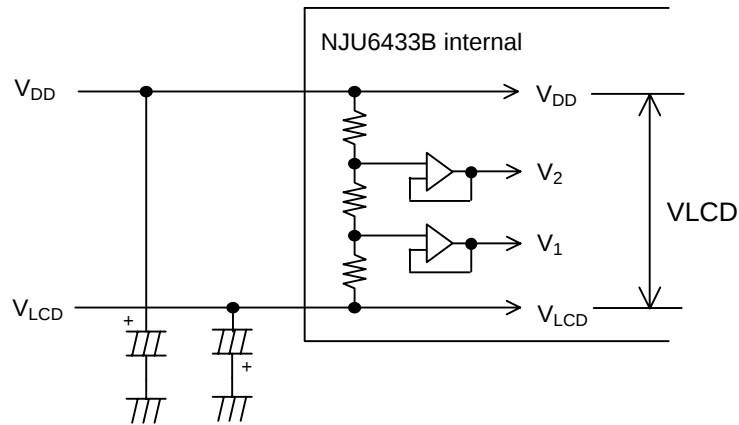
1. Mode setting release (nonselective status)
2. Shift register : all "0"
3. Latch circuit : all "0"



(6) LCD Panel Drive

(6-1) LCD driving voltage generation circuit

The LCD driving voltage generation circuit generates LCD driving bias voltages V_1 and V_2 from input voltage V_{DD} - V_{LCD} . It is generated by the bleeder resistance in IC, and after impedance is converted by the voltage follower, it is supplied to the LCD driving circuit. The V_{DD} and V_{LCD} terminal requires external capacitors for bias voltage stabilization for display quality as shown in below.



■ ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Operating Voltage (1)	V_{DDmax}	V_{DD} Terminal, Ta=25°C	-0.3~+7.0	V
Operating Voltage (2)	V_{LCD}		$V_{DD}-6.5 \sim V_{SS}$	V
Input Voltage (1)	$V_{1(1)}$	CE, SCL, DATA, MODE, INHb Terminals Ta=25°C	-0.3~+7.0	V
Input Voltage (2)	$V_{1(2)}$	OSC ₁ , OSC ₂ Terminals	-0.3~ $V_{DD}+0.3$	V
Output Voltage	V_O	OSC ₁ , OSC ₂ Terminals	-0.3~ $V_{DD}+0.3$	V
Output Current (1)	$I_{O(1)}$	SEG ₁ ~SEG ₅₀ Terminals	100	μA
Output Current (2)	$I_{O(2)}$	COM ₁ ~COM ₄ Terminals	1.0	mA
Power Dissipation	P_{Dmax}	Ta=85°C	300	mW
Operating Temperature	T_{opr}		-30~+85	°C
Storage Temperature	T_{stg}		-40~+125	°C

Note 1) All voltage values are specified as $V_{SS} = 0V$.

Note 2) If the LSI is used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 3) The relation $V_{DD} > V_{SS} \geq V_{LCD}$ must be maintained.

Note 4) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the LSI.

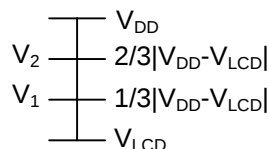
■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

($V_{DD}=5V \pm 10\%$, $V_{LCD}=V_{DD}-6.5V$, Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT	NO TE
Operating Voltage (1)	V _{DD}	V _{DD} Terminal		2.4	5.0	5.5	V	
Operating Voltage (2)	V _{LCD}	V _{LCD} Terminal		V _{SS}		V _{DD} -6.5	V	
"H" Input Voltage	V _{IH}	CE, SCL, DATA, MODE, INHb		0.7V _{DD}		V _{DD}	V	
"L" Input Voltage	V _{IL}			V _{SS}		0.3V _{DD}	V	
"H" Input Current	V _{IH}	CE,SCL, DATA,MODE, INHb	V _I =V _{DD}			5	uA	
"L" Input Current	V _{IL}		V _I =V _{SS}			5	uA	
"H" Output Voltage (1)	V _{OH(1)}	SEG ₁ ~SEG ₅₀	I _O =-10uA	V _{DD} -1.0			V	
"L" Output Voltage (1)	V _{OL(1)}		I _O =+10uA			V _{LCD} +1.0	V	
Middle Level Voltage 1/3(1)	V _{MS1/3}	SEG ₁ ~SEG ₅₀	I _O =±10uA	V ₁ -1.0	V ₁	V ₁ +1.0	V	1
Middle Level Voltage 2/3(1)	V _{MS2/3}		I _O =±10uA	V ₂ -1.0	V ₂	V ₂ +1.0	V	
"H" Output Voltage (2)	V _{OH(2)}	COM ₁ ~COM ₄	I _O =-100uA	V _{DD} -0.6			V	
"L" Output Voltage (2)	V _{OL(2)}		I _O =+100uA			V _{LCD} +0.6	V	
Middle Level Voltage 1/3(2)	V _{MC1/3}	COM ₁ ~COM ₄	I _O =±100uA	V ₁ -0.6	V ₁	V ₁ +0.6	V	1
Middle Level Voltage 2/3(2)	V _{MC2/3}		I _O =±100uA	V ₂ -0.6	V ₂	V ₂ +0.6	V	
Oscillating Frequency Range	f _{RNG}	OSC ₁ , OSC ₂ Terminals		25		200	kHz	
Oscillating Frequency	f _{OSC}	OSC ₁ , OSC ₂ Terminals R=140kΩ, V _{DD} =5V		115	130	145	kHz	
Operating Current (1)	I _{SS}	V _{SS} Terminal, V _{DD} =5V			50	80	uA	
Operating Current (2)	I _{LCD}	V _{LCD} Terminal, V _{DD} =5V, V _{LCD} =V _{DD} -6.5V			15	25	uA	
Hysteresis Voltage	V _H	CE, SCL, DATA, MODE, INHb V _{DD} =5V		0.3			V	

Note 1) $V_1=1/3|V_{DD}-V_{LCD}|$, $V_2=2/3|V_{DD}-V_{LCD}|$

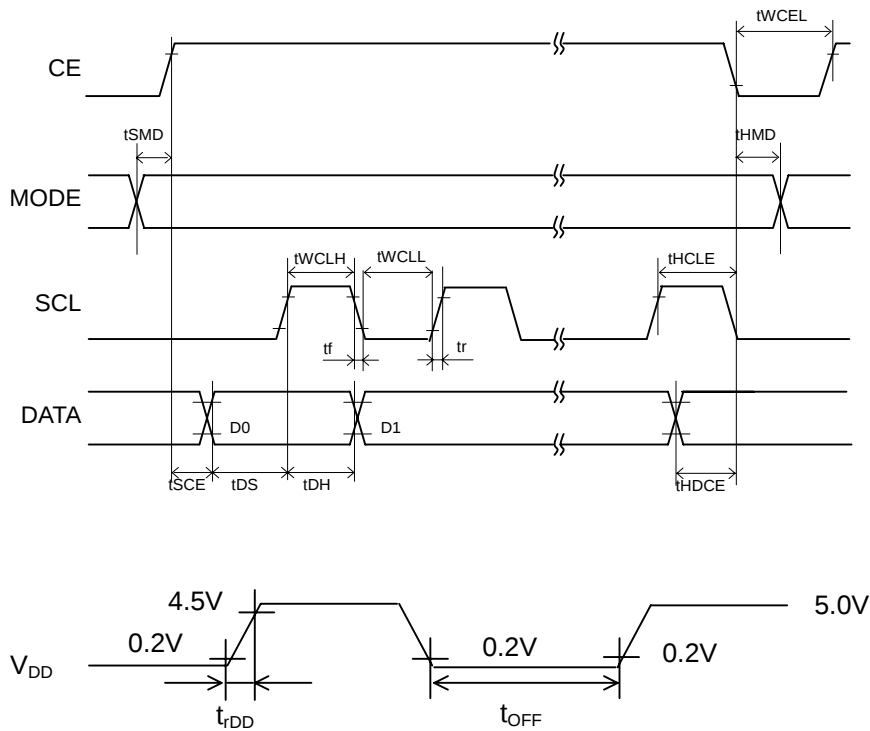


AC Characteristics

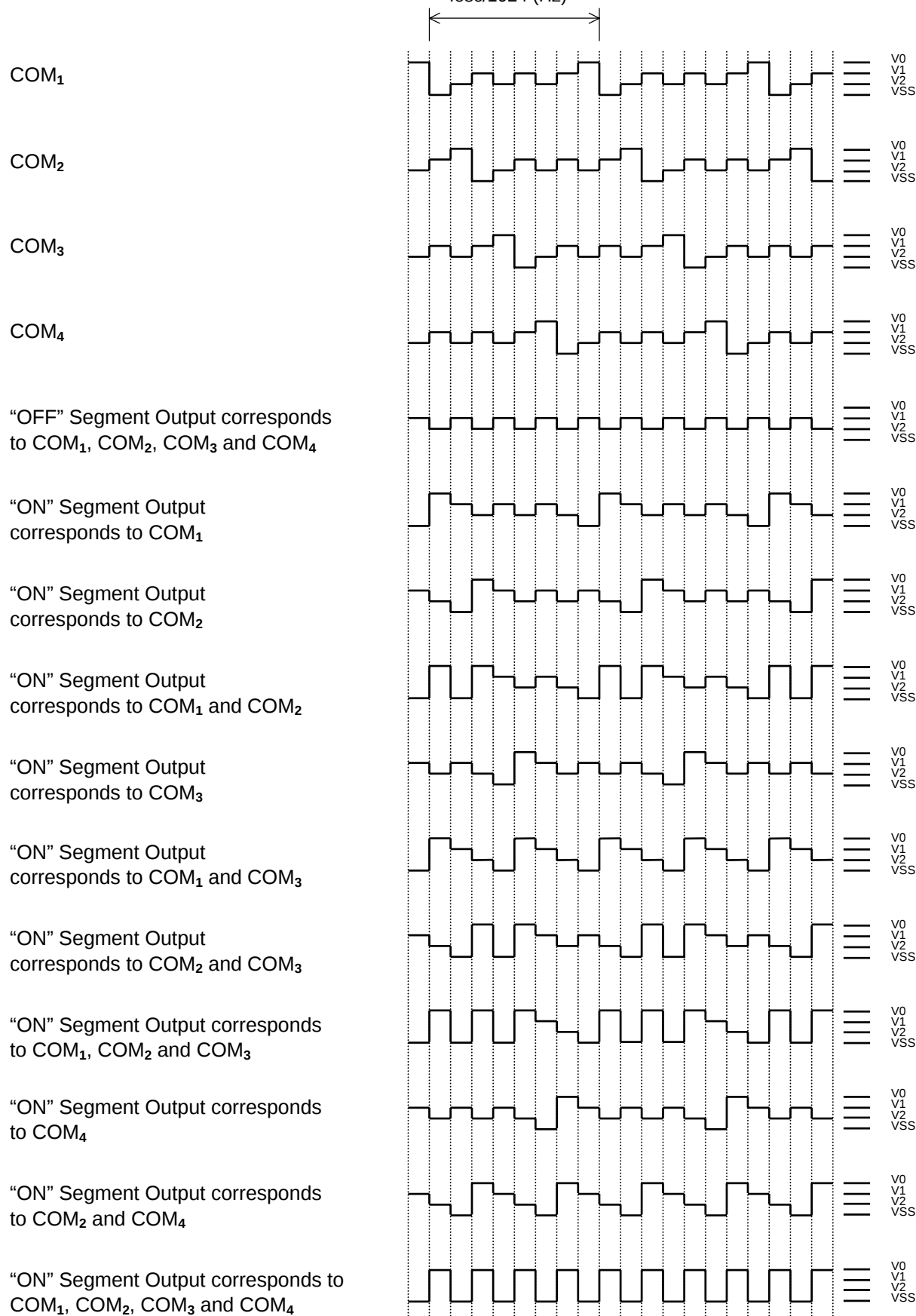
($V_{DD}=5V\pm10\%$, $T_a=25^\circ C$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
"L" Clock Pulse Width	t_{WCLL}	SCL	0.25			μs
"H" Clock Pulse Width	t_{WCLH}	SCL	0.25			μs
DATA Set-up Time	t_{DS}	SCL, DATA	0.25			μs
DATA Hold Time	t_{DH}	SCL, DATA	0.25			μs
CE Set-up Time	t_{SCE}	CE, DATA	1.0			μs
CE Hold Time (1)	t_{HDCE}	CE, DATA	1.0			μs
CE Hold Time (2)	t_{HCLE}	CE, SCL	1.25			μs
MODE Set-up Time	t_{SMD}	MODE, CE	0.25			μs
MODE Hold Time	t_{HMD}	MODE, CE	0.25			μs
"L" Chip Enable Pulse Width	t_{WCEL}	CE	4.0			μs
Rise Time	t_r	SCL			50	ns
Fall Time	t_f	SCL			50	ns
Power Supply Rise Time	t_{rDD}	V_{DD}	0.1		10	ms
Power Supply OFF Time	t_{OFF}	V_{DD}	1			ms

Input Timing Characteristics



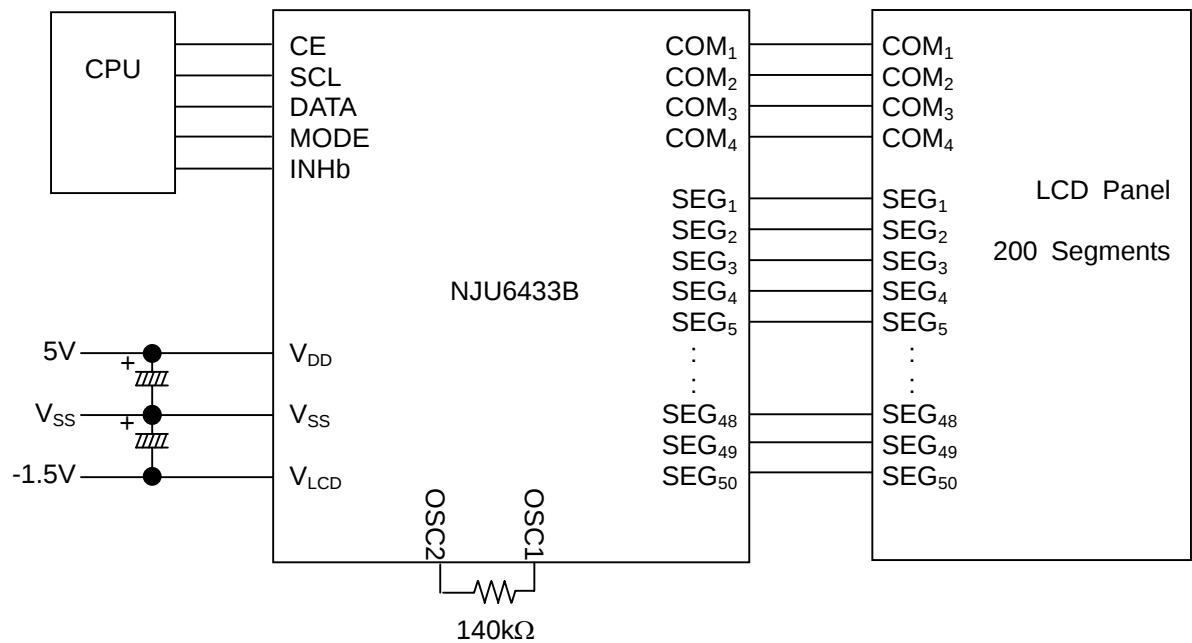
- LCD Driving Waveform(1/4DUTY · 1/3BIAS)

$$1\text{frame} = f_{\text{osc}}/1024 \text{ (Hz)}$$


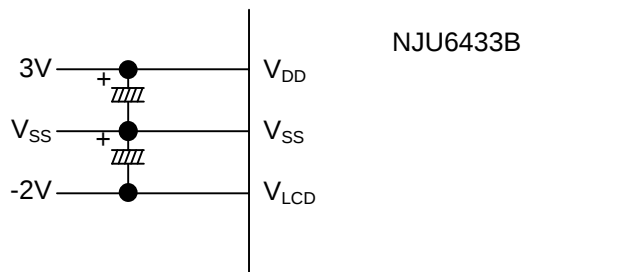
NJU6433B

APPLICATION CIRCUIT

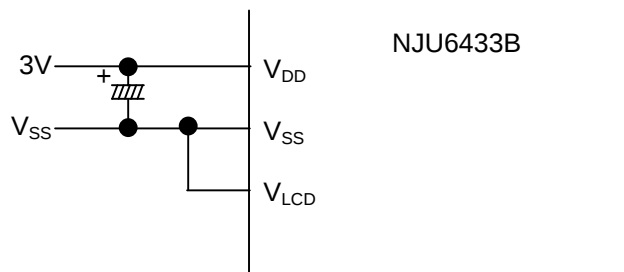
Example) VDD=5V, VLCD=6.5V



Example) VDD=3V, VLCD=5V



Example) VDD=3V, VLCD=3V



[CAUTION]
The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.